Prescaled Counters
in FLEX 8000 Devices

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Summary

Files using the techniques described in this application brief are available from the Altera BBS at (408) 954-0104 in the following self-extracting file:

ab_124.exe

Prescaled counters are counters that are specifically designed for high-frequency counting. Prescaled counters achieve their high performance because only the least significant bits (LSBs) transition at higher frequencies, while the most significant bits (MSBs) have more time to prepare for their transitions. FLEX 8000 devices can implement prescaled counters at frequencies of up to 142.9 MHz for counters of up to 16 bits. Design techniques described in this application brief can be used to create design files optimized for the following characteristics:

Design Goals:		*Design Results:*		
Architecture	**Optimization**	**Width**	**Logic Cells**	**Speed (MHz)**
✓ Look-Up Table	Routability	8 Bits	37	142.9
Product Term	✓ Speed	16 Bits	101	142.9
	Area	32 Bits	–	–

Prescaled Counters

Figure 1 shows a single bit of a prescaled counter implemented in a FLEX8000 device. When binary counters are clocked, each counter bit is driven low if all of its LSBs are high. However, since all but the LSB will have been high in the previous Clock cycle, the performance-critical path is from the LSBs (Q0) to all other register bits. In fact, the MSBs will have been high for several Clock cycles.

To achieve the maximum possible counting frequencies, the loading of prescaled counters occurs outside of the speed-critical path. With this implementation, synchronous loading of a prescaled counter requires multiple Clock cycles. Loading functions are typically not required but are frequently used to divide very-high-speed incoming Clocks.

To achieve the highest performance, the two LSBs (Q0 and Q1) are repeated in each Logic Array Block (LAB) of this counter. By replicating these bits, the only interconnect delay in the performance-critical path is the local LAB interconnect of 1ns. Thus, the speed-critical path for each bit requires only 7 ns (or 142.9 MHz). When fast Clock speed is the most important consideration, you can use additional logic resources to ensure the maximum possible performance.

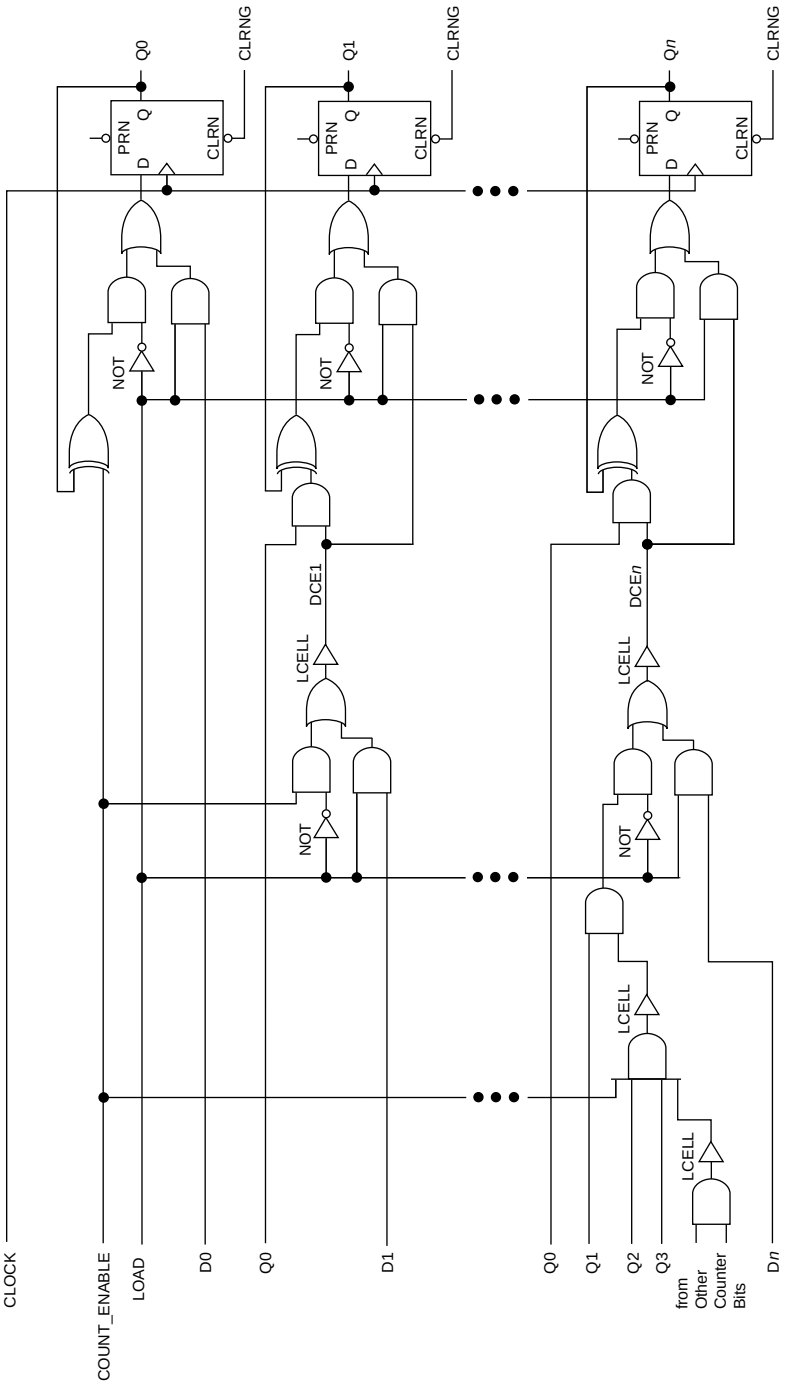

Figure 1. Single-Bit Prescaled Counter